What is claimed is:

1. A method of manufacturing a semiconductor integrated circuit having a first circuit region using a first power supply voltage and a second circuit region using a second power supply voltage different from said first power supply voltage wherein:

a first design rule is applied to said first circuit region in accordance with said first power supply voltage; and

a second design rule is applied to said second circuit region in accordance with said second power supply voltage.

2. The method of manufacturing the semiconductor integrated circuit as claimed in claim 1, wherein:

a wiring interval of said first circuit region is determined as a minimum distance allowing a first breakdown voltage of said first design rule; and

a wiring interval of said second circuit region is determined as a minimum distance allowing a second breakdown voltage of said second design rule.

3. The method of manufacturing the semiconductor integrated circuit as claimed in claim 1, wherein:

a distance between adjacent two vias formed in said first circuit region is determined as a minimum distance allowing a first breakdown voltage of said first design rule; and

a distance between adjacent two vias formed in said second circuit region is determined as a minimum distance allowing a second breakdown voltage of said second design rule.

4. The method of manufacturing the semiconductor integrated circuit as claimed in claim 3, wherein:

said distance between the adjacent two vias formed in said first circuit region is the shortest distance therebetween; and

said distance between the adjacent two vias formed in said second circuit region is the shortest

distance therebetween.

5. The method of manufacturing the semiconductor integrated circuit as claimed in claim 1, wherein:

a distance between adjacent wiring groove and via formed in said first circuit region is determined as a minimum distance allowing a first breakdown voltage of said first design rule; and

a distance between adjacent wiring groove and via formed in said second circuit region is determined as a minimum distance allowing a second breakdown voltage of said second design rule.

6. The method of manufacturing the semiconductor integrated circuit as claimed in claim 5, wherein:

said distance between the adjacent wiring groove and via formed in said first circuit region is the shortest distance therebetween; and

said distance between the adjacent wiring groove and via formed in said second circuit region is the shortest distance therebetween.

7. The method of manufacturing the semiconductor integrated circuit as claimed in claim 1, wherein said semiconductor integrated circuit employs a Dual-Damascene process to form metal wirings of said first and second circuit regions.

8. The method of manufacturing the semiconductor integrated circuit as claimed in claim 7, wherein said metal wirings are copper wirings.

9. A semiconductor integrated circuit having a first circuit region using a first power supply voltage and a second circuit region using a second power supply voltage different from said first power supply voltage wherein:

said first circuit region is manufactured by a first design rule in accordance with said first power supply voltage; and

said second circuit region is manufactured by a second design rule in accordance with said second

power supply voltage.

10. The semiconductor integrated circuit as claimed in claim 9, wherein:

said first circuit region has a first wiring interval corresponding to a minimum distance allowing a first breakdown voltage of said first design rule; and

said second circuit region has a second wiring interval corresponding to a minimum distance allowing a second breakdown voltage of said second design rule.

11. The semiconductor integrated circuit as claimed in claim 9, wherein:

said first circuit region has a first distance between adjacent two vias formed in said first circuit region corresponding to a minimum distance allowing a first breakdown voltage of said first design rule; and

said second circuit region has a second distance between adjacent two vias formed in said second circuit region corresponding to a minimum distance allowing a second breakdown voltage of said second design rule.

12. The semiconductor integrated circuit as claimed in claim 11, wherein:

said first distance is the shortest distance between the adjacent two vias formed in said first circuit region; and

said second distance is the shortest distance between the adjacent two vias formed in said second circuit region.

13. The semiconductor integrated circuit as claimed in claim 9, wherein:

said first circuit region has a first distance between adjacent wiring groove and via formed in said first circuit region corresponding to a minimum distance allowing a first breakdown voltage of said first

design rule; and

said second circuit region has a second distance between adjacent wiring groove and via formed in said second circuit region corresponding to a minimum distance allowing a second breakdown voltage of said second design rule.

14. The semiconductor integrated circuit as claimed in claim 13, wherein:

said first distance is the shortest distance between the adjacent wiring groove and via formed in said first circuit region; and

said second distance is the shortest distance between the adjacent wiring groove and via formed in said second circuit region.

15. The semiconductor integrated circuit as claimed in claim 9, wherein said semiconductor integrated circuit employs a Dual-Damascene process to form metal wirings of said first and second circuit regions.

16. The semiconductor integrated circuit as claimed in claim 15, wherein said metal wirings are copper wirings.